DMEA SBIR 14.2 PROPOSAL SUBMISSION INSTRUCTIONS

INTRODUCTION

The Defense Microelectronics Activity (DMEA) SBIR Program is implemented, administrated, and managed by the DMEA Program Control Division. If you have any questions regarding the administration of the DMEA SBIR Program, please contact the DMEA SBIR Program Manager (PM), Mr. Kevin Rankin, kevin.rankin@dmea.osd.mil.

For general inquiries or problems with electronic submission, contact the DoD SBIR Help Desk at 1-866-724-7457 (1-866-SBIRHLP) between 8:00 am to 5:00 pm ET. For questions about the topic during the pre-solicitation period (23 April 2014 through 22 May 2014), contact the Topic Authors listed under each topic on the http://www.dodsbir.net/ Web site prior to the solicitation. Information regarding the DMEA mission and programs can be found at http://www.dmea.osd.mil.

PHASE I GUIDELINES

DMEA intends for Phase I to be only an examination of the merit of the concept or technology that still involves technical risk, with a cost not exceeding \$150,000.

A list of the topics currently eligible for proposal submission is included in this section followed by full topic descriptions. These are the only topics for which proposals will be accepted at this time. The topics are directly linked to DMEA's core research and development requirements.

Please assure that your e-mail address listed in your proposal is current and accurate. DMEA cannot be responsible for notification to companies that change their mailing address, e-mail address, or company official after proposal submission.

PHASE I PROPOSAL SUBMISSION

Read the DoD front section of this solicitation for detailed instructions on proposal format and program requirements. When you prepare your proposal submission, keep in mind that Phase I should address the feasibility of a solution to the topic. Only UNCLASSIFIED proposals will be entertained. DMEA accepts Phase I proposals not exceeding \$150,000. The technical period of performance for the Phase I should be no more than 6 months. DMEA will evaluate and select Phase I proposals using the evaluation criteria contained in Section 6.0 of the DoD Solicitation 14.2 preface. Due to limited funding, DMEA reserves the right to limit awards under any topic and only proposals considered to be of superior quality will be funded.

If you plan to employ NON-U.S. citizens in the performance of a DMEA SBIR contract, please identify these individuals in your proposal as specified in Section 5.4.c(8) of the program solicitation.

It is mandatory that the <u>ENTIRE</u> Technical Volume, DoD Proposal Cover Sheet, Cost Volume and the Company Commercialization Report are submitted electronically through the DoD SBIR Web site at http://www.dodsbir.net/submission. If you have any questions or problems with the electronic proposal submission contact the DoD SBIR Helpdesk at 1-866-724-7457.

This <u>COMPLETE</u> electronic proposal submission includes the submission of the Cover Sheets, Cost Volume, Company Commercialization Report, the ENTIRE Technical Volume and any appendices via

the DoD Submission site. The DoD proposal submission site http://www.dodsbir.net/submission will lead you through the process for submitting your technical proposal and all of the section electronically. Each of these documents is submitted separately through the Web site. Your proposal submission must be submitted via the submission site on or before the 6:00 a.m. deadline on 25 June 2014. https://www.dodsbir.net/submission will lead you through the section electronically. Each of these documents is submission site on or before the 6:00 a.m. deadline on 25 June 2014. Proposal submissions received after the closing date and time will not be considered.

PHASE II GUIDELINES

Phase II is the prototype/demonstration of the technology that was found feasible in Phase I. DMEA encourages, but does not require, partnership and outside investment as part of discussions with DMEA sponsors for potential Phase II efforts.

Phase II proposals may be submitted for an amount not to exceed \$1,000,000.

PHASE II PROPOSAL SUBMISSION

The Reauthorization of the SBIR/STTR Program has resulted in significant changes to the Phase II proposal submission process. On December 31, 2011, the President of the United States signed into law the National Defense Authorization Act for Fiscal Year 2012 (Defense Reauthorization Act), Public Law 112–81. Section 5001, Division E, of the Defense Reauthorization Act contains the SBIR/STTR Reauthorization Act of 2011 (SBIR/STTR Reauthorization Act), which extends both the SBIR and STTR Programs through September 30, 2017.

Phase I awardees may submit a Phase II proposal without invitation not later than thirty (30) calendar days following the end of the Phase I contract. The DMEA SBIR Contracting Officer will provide additional instructions to each of the Phase I awardees before the end of their respective Phase I contract completion dates.

All Phase II proposals must have a complete electronic submission. Complete electronic submission includes the submission of Cover Sheet, Cost Volume, Company Commercialization Report, the entire Technical Volume, and any appendices via the DoD submission site (http://www.dodsbir.net/submission). The DoD proposal submission site will lead you through the process for submitting your technical volume and all of the sections electronically. Each of these documents is submitted separately through the Web site. Your proposal must be submitted via the submission site on or before the DMEA-specified deadline or it will not be considered.

DMEA will evaluate Phase II proposals based on the Phase II evaluation criteria listed in Section 8.0 of the solicitation preface.

COST VOLUME GUIDELINES

The on-line cost volume for Phase I and Phase II proposal submissions must be at a level of detail that would enable DMEA personnel to determine the purpose, necessity, and reasonability of each cost element. Provide sufficient information (a through i below) on how funds will be used if the contract is awarded. Include the itemized cost volume information (a through i below) as an appendix in your technical proposal. The itemized cost volume information (a through i below) will <u>not</u> count against the 20-page limit.

a. Special Tooling and Test Equipment and Material: The inclusion of equipment and materials will be carefully reviewed relative to need and appropriateness of the work proposed. The purchase of special tooling and test equipment must, in the opinion of the Contracting

Officer, be advantageous to the government and relate directly to the specific effort. They may include such items as innovative instrumentation and/or automatic test equipment. Title to property furnished by the Government or acquired with Government funds will be vested with the DoD Component, unless it is determined that transfer of the title to the contractor would be more cost effective than recovery of the equipment by the DoD Component.

- b. Direct Cost Materials: Justify costs for materials, parts, and supplies with an itemized list containing types, quantities, price, and where appropriate, purposes.
- c. Other Direct Costs: This category of costs includes specialized services such as machining or milling, special testing or analysis, costs incurred in obtaining temporary use of specialized equipment. Proposals, which include teased hardware, must provide an adequate lease *versus* purchase justification or rationale.
- d. Direct Labor: Identify key personnel by name if possible or by labor category if specific names are not available. The number of hours, labor overhead and/or fringe benefits and actual hourly rates for each individual are also necessary.
- e. Travel: Travel costs must relate to the needs of the project. Break out travel cost by trip, with the number of travelers, airfare, and per diem. Indicate the destination, duration, and purpose of each trip.
- f. Cost Sharing: Cost sharing is permitted. However, cost sharing is not required, nor will it be an evaluation factor in the consideration of a proposal.
- g. Subcontracts: Involvement of university or other consultants in the planning and /or research stages of the project may be appropriate. If the offeror intends such involvement, describe the involvement in detail and include information in the cost proposal. The proposed total of all consultant fees, facility leases, or usage fees and other subcontract or purchase agreements may not exceed one-third of the total contract price or cost, unless otherwise approved in writing by the Contracting Officer. Support subcontract costs with copies of the subcontract agreements. The supporting agreement documents must adequately describe the work to be performed (i.e., Cost Volume). At the very least, a statement of work with a corresponding detailed cost volume for each planned subcontract must be provided.
- h. Consultants: Provide a separate agreement letter for each consultant. The letter should briefly state what service or assistance will be provided, the number of hours required, and the hourly rate.

DMEA SBIR PHASE II ENHANCEMENT PROGRAM

To encourage transition of SBIR into DoD systems, DMEA has a Phase II Enhancement policy. DMEA's Phase II Enhancement program requirements include: up to one year extension of existing Phase II, and up to \$500,000 matching SBIR funds. Applications are subject to review of the statement of work, the transition plan, and the availability of funding. DMEA will generally provide the additional Phase II Enhancement funds by modifying the Phase II contract.

PHASE I PROPOSAL SUBMISSION CHECKLIST:

All of the following criteria <u>must be met</u> or your proposal will be REJECTED.

1. Your Tech	mical Volume, the DoD Cover Sheet, the DoD Company Commercialization
Report (required e	ven if your firm has no prior SBIRs), and the Cost Volume have been submitted
electronically thro	ugh the DoD submission site by 6:00 am ET on 25 June 2014.
2. The Phase	I proposal does not exceed \$150,000.

DMEA SBIR 14.2 Topic Index

DMEA142-001

Quantum Cryptography Single Photon Detector Chip

DMEA SBIR 14.2 Topic Descriptions

DMEA142-001 TITLE: Quantum Cryptography Single Photon Detector Chip

TECHNOLOGY AREAS: Materials/Processes, Sensors, Electronics

The technology within this topic is restricted under the International Traffic in Arms Regulation (ITAR), which controls the export and import of defense-related material and services. Offerors must disclose any proposed use of foreign nationals, their country of origin, and what tasks each would accomplish in the statement of work in accordance with section 5.4.c.(8) of the solicitation.

OBJECTIVE: Develop a single photon detector/counting chip consisting of an Avalanche Photodiode (APD) and accompanying electronics manufactured on a transparent substrate IC process for use in a secure fiber optic communications link.

DESCRIPTION: Fifteen thousand DoD networks with seven million devices at 4,000 installations in 88 countries are being eavesdropped upon over a million times a day [1]. Clearly, computers are getting faster and more powerful every year (Moore's Law) so the bar constantly needs to be set higher to secure electronic transmission from would-be hackers. Crimes connected to ATMs and online transactions are on the rise. Cryptology is the science of secure communication and relies on various mathematical algorithms to create difficult encryption (the process of encoding information such that only the computer with the 'key' can decode it). Unfortunately, in digital cryptography, an intruder's attack can be undetectable. The intruder can intercept messages unnoticed and then perform extensive computer analysis off-line. There is no defense against this type of interception [2].

Quantum cryptography applies an encryption scheme that uses a series of single, polarized photons that act as the 'key' between the sender and receiver. If an eavesdropper or would-be hacker tries to intercept this 'key,' these photons will immediately become corrupted, render the message unintelligible, and alert the sender and intended recipient to the spying attempt. Both users will postpone sending any valuable data until the optical link is secured [2] [3].

A secure communication quantum cryptography fiber-optic link consists of an LED or laser capable of transmitting single photons and associated electronics, a fiber optic channel and a detector capable of detecting or counting single photons. One of the hurdles and shortcomings of quantum cryptography has been the limited distance for transmission. In quantum cryptography, the sensitivity of the detector plays an important role in channel length. Hence, efforts are needed to engineer a highly sensitive detector with low noise and high efficiency [4].

An APD, which is designed using an appropriate IC manufacturing process, may be used in a secure communication link (quantum cryptography) for long distances. The IC process used, e.g. Silicon-On-Sapphire, must have a substrate that is transparent to optical wavelengths that are suitable for optoelectronic devices. Combining the appropriate fabrication process with the design of an APD will enable the development of a single photon detector capable of detecting polarized 'key' data over long distances [5] [6] [7].

The optimal solution will approach or exceed the following performance metrics:

- 100% detection of single photons ('keys') at a distance of 200km.
- Quantum efficiency of 85% or greater for the selected carrier wavelengths.
- Maximum single photon counting rate of 10 MHz.

PHASE I: The goal of Phase I is to develop a detector chip architecture with applications toward secure communication, namely quantum cryptography. These applications should have DoD-wide impact and relate to commercial applications as well. In developing the chip architecture, trade-offs between power, noise, data rate and sensitivity will be considered. Cost tradeoffs between available IC processes will also be determined. Computer simulations of the proposed detector architecture will also be performed to validate the selected architecture. In addition, data sets from real world platforms will be investigated to verify the validity of the proposed architecture. The chip architecture will support the sensory inputs of the potential application platforms and the outputs required for integration into a secure communication link. At the conclusion of this phase, a report that includes the above

mentioned requirements and program plan will be completed for chip development and initial application selection.

PHASE II: Phase II will result in a demonstration of a prototype version of the chip whose architecture was developed in Phase I. A final testing application will be selected, and data from the real world platform will be collected for chip performance simulations and testing in the lab before being transitioned to a real world platform. In conjunction with the demonstration, a detailed plan for taking the design to a production-level chip will be prepared.

PHASE III: Phase III will conclude with the chip design being implemented in Silicon-on-Sapphire. Integration and testing will be conducted on the target platform. Additional government and commercial customers for the chip will be identified.

POTENTIAL DUAL USE APPLICATIONS: This chip may be integrated into any commercial or DoD application requiring secure communication such as financial institutions, Social Security offices, doctors' offices, internet online purchases, classified weapons data, equipment frequencies, etc.

REFERENCES:

- 1. W. Jackson, "DoD Struggles to define Cyber War," Defense Systems Knowledge Technologies and Net-Enabled Warfare, May 12, 2010, http://www.defensesystems.com/Articles/2010/05/12/Miller-on-Cyberwar-051210.aspx.
- 2. ICinnovation website, http://www.icinnovation.nl/emerging-technologies/nanotechnology/quantum-cryptography.html.
- 3. Research and Markets website, http://www.frost.com/prod/servlet/report-brochure.pag?id=D345-01-00-00-00.
- 4. R. Pizzi, "Prototype of a Quantum Cryptography System for the End User," Proceedings of the 9th WSEAS International Conference on Applied Computer Science, Oct 17-19, 2009, http://www.dti.unimi.it/pizzi/files%20nuove%20pubblicazioni/WSEAS%20CRYPTO.pdf.
- 5. E. Culurciello, "16x16 Pixel Silicon on Sapphire CMOS Digital Pixel Photosensor Array," IEEE Electronics Letter, Jan 8, 2004, Vol. 40, No. 1.
- 6. F. Zappa, "Integrated Array of Avalanche Photodiodes for Single-Photon Counting," Proceeding of the 27th European Solid-State Device Research Conference, Sep22-24, 1997.
- 7. A.G. Stern, "High Quantum Efficiency, Back-Illuminated, Crystallographically Etched, Silicon-on-Sapphire Avalanche Photodiode with Very Wide Dynamic Range, for Manufacturable High Resolution Imaging Arrays," SPIE Proceedings, Jan 27, 2009, Vol. 7249.

KEYWORDS: Single-Photon Detector, Optical Cryptography, SOS, Avalanche Photodiode (APD), Photon Detector

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